Paper review of
"Hardware-Oriented Algorithm for Cube Root Calculation"
by Duque-Villegas and Velasco-Medina

The major value of this paper is the implementation of Peng's algorithm [1] on an FPGA and evaluating its performance. Peng's 1981 algorithm was applied as peripheral equipment to the Chinese DJS-130 minicomputer. According to Wikipedia, early FPGAs wouldn't become available until 1984. In referencing Peng's work, this paper states that "however, those algorithms include multiplication operations, which require more processing time and area resources." Peng also identifies multiplication as an issue and designs his cube root algorithm to use shifts and adds as is done in this paper.

The algorithm described seems to be Peng's algorithm. This paper's foundational equation (6) is similar to Peng's equation (8) and equation (9) to Peng's equation (10).

This paper used the Area-Time (A*T) metric to demonstrate the optimality cube root algorithms. The Putra and Adiono paper [2] evaluates their algorithm on four FPGAs and show a 2.3 times variance in the Area-Time metric (Table 1). Papers [4] and [5] also use the Area-Time metric, but use nand gate count versus LE/LUTs, which provides a better representation of area.

	Altera		Xilinx	
Family	Cyclone II	Stratix II	Spartan 6	Virtex 5
Area (A)	429 LEs + 121 Reg = 550	288 ALUTs + 121 Reg = 409	415 LUTs + 121 Reg = 536	380 LUTs + 121 Reg = 501
# clock cycle	13	13	13	13
Freq(MHz)	54.60	72.81	40.09	69.01
Period (ns)	18.32ns	13.73ns	24.94ns	14.49ns
Time (T)	238.16ns	178.49ns	324.22ns	184.47ns
A*T	130,988	73,002	169,567	92,419

Table 1

A paper not reference is Yi and Chu's cube root [3]. They optimized their algorithm by eliminating multiplications, calculating the square in advance, and using carry-save adders. In comparing the Area-Time metric with this algorithm it shows almost a two-fold improvement over that of this paper's (Table 2), but we know this metric is not meaningful across different platforms.

	This Paper	Yi & Chu [3]
Family	Cyclone V	Cyclone IV
Area (A)	205 ALUTs + 105 Reg = 310	298 LEs + 109 Reg = 407
# clock cycle	42	11
Freq(MHz)	217.86	147.47
Period (ns)	4.59ns	6.78ns
Time (T)	192.78ns	74.59ns
A*T	59,762	30,358

Table 2

The paper made a valuable attempted to compare the optimality of cube root algorithms, but as the data shows, comparisons cannot be made across FPGA platforms. If one did a test of various algorithms on a single platform, that would be valuable contribution, providing insights that are currently unavailable.

[1] H. Peng, "Algorithms for extracting square roots and cube roots," 1981 IEEE 5th Symposium on Computer Arithmetic (ARITH), Ann Arbor, MI, USA, 1981, pp. 121-126.

[2] R. V. W. Putra and T. Adiono, "Optimized hardware algorithm for integer cube root calculation and its efficient architecture," 2015 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), Nusa Dua, 2015, pp. 263-267.

[3] Y. Li and W. Chu, "On the improved implementations and performance evaluation of digit-by-digit integer restoring and non-restoring cube root algorithms," 2016 International Conference on Computer, Information and Telecommunication Systems (CITS), Kunming, 2016, pp. 1-5.

[4] A. Pineiro, J. D. Bruguera, F. Lamberti and P. Montuschi, "A Radix-2 Digit-by-Digit Architecture for Cube Root," in IEEE Transactions on Computers, vol. 57, no. 4, pp. 562-566, April 2008.

[5] A. Va´zquez and J. D. Bruguera, "Composite Iterative Algorithm and Architecture for q-th Root Calculation," 2011 IEEE 20th Symposium on Computer Arithmetic, Tubingen, 2011, pp. 52-61.